	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	2558	address$3 with priorit$3 with (stor$3 or buffer$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/09 16:17
2	BRS	L2	681	address$3 with reorder$3 with (store or memory or buffer$3)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/09 16:12
3	BRS	L3	148	address$3 adj3 priorit$3 adj3 (stor$3 or buffer$3 or memory)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/09 16:12
4	BRS	L4	78	address$3 adj2 priorit$3 adj2 (stor$3 or buffer$3 or memory)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2004/06/09 16:13

US-PAT-NO: 6157987

DOCUMENT-IDENTIFIER: US 6157987 A

TITLE: Pixel engine data caching mechanism

DATE-ISSUED: December 5, 2000

US-CL-CURRENT: 711/129, 345/422 , 345/506 , 345/543 , 345/557 , 345/582
, 711/136 , 711/137 , 711/173

APPL-NO: 08/ 976748

DATE FILED: November 24, 1997

PARENT-CASE:

This is a divisional of application Ser. No. 08/616,540, filed Mar. 15,
1996, now U.S. Pat. No. 5,761,720.

--------- KWIC --------

Detailed Description Text - DETX (24):

As described above, address computation/allocation circuitry 535 is notified
of the direction in which memory is being accessed with direction signal 313B.
As shown in FIG. 5, after address computation/allocation circuitry 535

determines the two memory addresses as well as prioritizes the two memory addresses, the highest priority memory address is output as first memory address 541. The other memory address, if needed, is output as second memory address 543. The two memory address signals 541 and 543 are received by tag comparison circuitry 537.

US-PAT-NO: 6298424

DOCUMENT-IDENTIFIER: US 6298424 B1

TITLE: Computer system including priorities for memory operations and allowing a higher priority memory operation to interrupt a lower priority memory operation

DATE-ISSUED: October 2, 2001

US-CL-CURRENT: 711/158, 711/137 , 711/151

APPL-NO: 09/ 522649

DATE FILED: March 10, 2000

PARENT-CASE:

This application is a continuation of U.S. patent application Ser. No.
08/982,588, filed on Dec. 2, 1997, now U.S. Pat. 6,058,461.

---------- KWIC ---------

Detailed Description Text - DETX (9):

By interrupting a lower priority memory operation to perform a higher
priority memory operation in the same page only, the higher priority memory
operation may be performed quickly (e.g. with a page hit timing). If

a
different page were accessed, then the current page would be deactivated and
the new page accessed by providing the row address of the higher priority
memory operation, then the corresponding column addresses. Subsequently, the
new page would be deactivated and the page corresponding to the lower priority
memory operation re-established. The time spent deactivating and activating
pages may outweigh the latency savings for the higher priority memory
operation.

Detailed Description Text - DETX (21):

Generally, control unit 46 may select memory operations from request queue
44 in order. However, a higher priority memory operation (as indicated via the
priority assigned to the memory operation by the master for the memory
operation) may be selected over a prior, lower priority memory operation (if
the lower priority memory operation is to a different address than the higher
priority memory operation). Control unit 46 conveys the address of the
selected memory operation to main memory 14 along with corresponding control
information via address and control bus 16A In the present embodiment, the
control information includes a write enable line to indicate that the operation
is a read or write, a row address strobe (RAS_) line to indicate that

the row portion of the address is being conveyed, and a column address strobe (CAS_) line to indicate that the column address is being conveyed. Other control lines may be included as well (for example, bank select lines for selecting which bank or banks is to respond to an access, etc.). The row portion of the address is conveyed first, along with an activation of the RAS_line. Subsequently, the column portion of the address is conveyed along with an activation of the CAS_line. If the operation is a read, the selected data is provided by main memory 14 upon data bus 16B. Data buffer 50 may capture the data from the data bus under the direction of control unit 46. If the operation is a write, the write data is driven by control unit 46 upon data bus 16B.

Detailed Description Text - DETX (23):

Control unit 46 records the page (e.g. the row portion of the address) and the priority level of the in-progress memory operation in open page/priority storage 48. If a higher priority memory operation is detected (by comparing the priority level stored in open page/priority storage 48 to the priority level of incoming memory operations), and if the incoming memory operation is to the same page as the in-progress memory operation (detected by comparing the page recorded in open page/priority storage 48), then the

in-progress data
transfer may be interrupted to perform the higher priority memory operation.
The column portion of the address of the higher priority memory operation is
presented, and the corresponding data transferred. Subsequently, the lower
priority (formerly in-progress) memory operation is completed by presenting the
column portion of the address corresponding to the next data to be transferred,
and by transferring the remaining data.